REMARKS

The Examiner rejected claims 1-32 under 35 U.S.C. §103(a) as being unpatentable over Rajassamy (USP 6,331,800) in view of Tsukamoto et al. (USP 5,930,269).

Applicants respectfully traverse the §103(a) rejections with the following arguments.

35 USC § 103 Rejections

As to claims 1 and 6, the Examiner states that "Radjassamy in figure 3 disclose or teach an integrated circuit comprising a first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308) for adjusting of clock edge rise/fall times between non-overlapping clock signals and thereby eliminate a race (see col. 1, lines 5-9). Further, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Radjassamy **do not explicitly** show or teach power (rails) applied separetly to each of the IC chips wherein each IC chips comprise latches and logic circuits. **However,** Tsukamoto et al. in figure 4 teach a testing system comprises a burn-in board (11) to be diagnosed, a control signal generator (12) includes clock generator (12a) generates a clock signal CLK, and supplies the clock signal CLK to the burn-in board via scan signal distributor (12b), a power distributor (13) for supplying electric power Vcc to the burn-in board and in figure 5 the burn-in board shows products (IC1 1/IC12/ICln, IC21/IC22/IC2n...) of a semiconductor integrated circuit device arranged in rows and columns on the burn-in board, and are electrically connected through contact pins and furthermore Power supply lines VCC1, VCC2 and VCCm (power rails) are respectively associated with the columns of products of semiconductor device and the products are powered with power potential Vcc and the ground potential supplied from the associated power supply lines VCC1 to VCCm (see col. 3, lines 55-67 and col. 4, lines 1-22). **Therefore,** it would have

been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsukamoto et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to diagnosis the products on the burn-in board without undesirable influence of a partially defective product and automatically classifies the products between the excellent group, the partially defective group an the defective group (see col. 9, lines 48-58)."

Applicants contend that claims 1 and 6 are not obvious in view of Rajassamy in view of Tsukamoto et al. because Rajassamy in view of Tsukamoto et al. does not teach or suggest every feature of claims 1 and. As a first example, Rajassamy in view of Tsukamoto et al. does not teach or suggest "a first power rail for supplying power to a first latch and a circuit." As a second example, Rajassamy in view of Tsukamoto et al. does not teach or suggest "a second power rail for supplying power to a second latch and a circuit."

Applicants respectfully point out that the combination of Rajassamy in view of Tsukamoto et al. does not teach what power supply of Rajassmy would be connected to what latch of Tsukamoto et al." and that the examiners stated motivation does not even hint at how to combine the references to produce Applicants invention.

Applicants maintain that the Examiner's remarks that "The connection between a power supply and a flip-flop necessarily requires a medium for wiring between connections and the wiring is analogous to the claimed power rails and the more flip-flops utilized in a circuit configuartion, the more the number of wiring or power rails involved" is not only incorrect and misleading (having more flip flops does not require more power rails, they could for example all be wired to the same power rail) but has no bearing on Applicants argument that without

showing latches in Tsukamoto et al., it is impossible to say how Tsukamoto et al. combined with Radjassmy produces the latch/power rail combinations Applicants claim.

Applicants contend that the Examiners remarks that " the power supply distribution block (19) supplies power directly or indirectly to the logic circuits, even with the absence of it, it is obvious that the prior art logic circuits cannot properly function without being powered by power supply means." merely indicates that the Examiner has assumed logic circuits exist somewhere in Tsukamoto et al. and has no bearing on Applicants argument that without showing latches Tsukamoto et al., it is impossible to say how Tsukamoto et al. combined with Radjassmy produces the latch/power rail combinations Applicants claim.

Applicants contend the Examiner has assumed a specific combination based on Applicants disclosure and not any teaching in the prior art in violation of Applicants and further contend that the Examiner has impermissibly used the Applicants' teaching to hunt through the prior art for the claimed elements.

Applicants believe the Examiners rejection of claims 1 and 6 is improper based on *Karsten Mfg. Corp. v. Cleveland Gulf Co.*, 242 F.3d 1376, 1385, 58 U.S.P,Q.2d 1286, 1293 (Fed. Cir. 2001) which states " In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching inn the prior art that would have led a person of ordinary skill in the art to select the references and combine them **in the way that would produce the claimed invention**" and *C.R. Bard, Inc.* v. M3 Sys., Inc, 157 F.3d 1340, 1352, 48 U.S.P.Q.2d 1225, 1232 (Fed. Cur. 1998) which state "no prior art provided a teaching, suggestion or motivation that a needle assembly should be made **with the structure shown and claimed** in the '056 patent", and stating that "a showing of a suggestion, teaching, or motivation

to combine the prior art references is an 'essential evidentiary component of an obviousness holding'."

Additionally, Applicants still contend that there is no motivation to modify Rajassamy with Tsukamoto et al. as the method used by Tsukamoto et al. when applied to Rajassamy does not result in the benefit stated. Applicants respectfully point out that Radjassamy is directed to a serial test method while Tsukamoto et al. is directed to a parallel test method (see Tsukamoto FIG. 5). The Examiner states that the motivation to modify Rajassamy with Tsukamoto et al. is "in order to diagnosis the products on the burn-in board without undesirable influence of a partially defective product and automatically classifies the products between the excellent group, the partially defective group an the defective group" The "undesirable influence" of Tsukamoto et al. is a power supply short to ground on a damaged I/O pin of one IC interacting with the signal generated on I/O pins of other I/Cs when the I/O pins of all ICs are coupled in parallel to a common data line (see and col. 2, lines 33-59). The logic circuits of Rajassamy are connected in series (see Rajassamy FIG. 3 and col. 1, lines 28-30). Rajassamy specifically tests for faults in a logic pattern clocked **serially** and a fault on one logic stage will propagate through all logic stages regardless of how power is supplied to the logic stages or latches of Rajassamy.

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 6 are not unpatentable over Radjassamy in view of Tsukamoto et al. and are in condition for allowance. Since claims 2-5 depend from claim 1, and claims 7-10 depend from claim 6, Applicants respectfully maintain that claims 2-5 and 7-10 are likewise in condition for allowance.

Applicants note that claim 11 includes all the elements of claim 1 and additionally adds limitations related to third and fourth power rails and that the Examiners stated reasons for

rejecting claim 11 is essentially identical to those given for rejecting claim 1. Therefore Applicants contend all of Applicants' arguments *supra* in respect to claims 1 and 6 are applicable to claim 11. Based on the preceding arguments, Applicants respectfully maintain that claim 11 is are not unpatentable over Radjassamy in view of Tsukamoto et al. and is in condition for allowance. Since claims 12-16 depend from claim 11, Applicants respectfully maintain that claims 12-16 are likewise in condition for allowance.

Applicants contend all of Applicants' arguments *supra* in respect to claims 1 and 6 are applicable to claims 17 and 22. Based on the preceding arguments, Applicants respectfully maintain that claims 17 and 22 are not unpatentable over Radjassamy in view of Tsukamoto et al. and are in condition for allowance. Since claims 18-21 depend from claim 17 and claims 23-26 depend from claim 22, Applicants respectfully maintain that claims 18-21 and 23-26 are likewise in condition for allowance.

Applicants contend that Applicants' arguments given *supra* in respect to claims 1 and 6 are applicable to claim 27. Based on the preceding arguments, Applicants respectfully maintain that claims 27 is not unpatentable over Radjassamy in view of Tsukamoto et al. and is in condition for allowance. Since claims 28-32 depend from claim 27, Applicants respectfully maintain that claims 28-32 are likewise not unpatentable over Radjassamy in view of Tsukamoto et al. and are in condition for allowance.

Applicants contend that the Examiner's rejection of and response to the Applicants' arguments for claims 3, 8, 13, 19 and 24 (repeated below) are even less legally persuasive, in that an even more specific combination of power supplies, power rails, clocks, latches and circuits are claimed in Applicants claims 3, 8, 13, 19 and 24 then are claimed in Applicants claims 1, 6, 11, 22 and 27.

Applicants contend that claims 3, 8, 13, 19 and 24 are not obvious in view of Radjassamy in view of Tsukamoto et al. because Radjassamy in view of Tsukamoto et al. does not teach or suggest every feature of claims 3, 8, 13, 19 and 24.

Using claim 1 as an example, the Examiner states "Radjassamy in view of Tsukamoto et al. teach all the subject matter claimed in claims 1 and 6 including Tsukamoto et al. in figure 5 teach plurality of burn-in products whereby each of the products connected by separate clocks (SCN1, SCN2...) and voltage lines VCC1, VCC2...)."

Applicants maintain, in the case of claim 3, Radjassamy in view of Tsukamoto et al. does not teach or suggest "said first and second clocks powered from a third power rail." Applicants point out that claim 3 specifically teach the clocks being powered from a different power supply than the power supply powering the latches and logic circuits. Rajassamy and Tsukamoto et al. are silent as to the source of the power for their clocks.

Applicants believe that the argument present for claim 3 is applicable to the Examiner's rejection of claims 8, 13, 19 and 24 as well and based on the preceding argument for claim 3, Applicants respectfully maintain that claims 3, 8, 13, 19 and 24 are not unpatentable over Radjassamy in view of Tsukamoto et al. and are in condition for allowance

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
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